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(54) **METHOD FOR FABRICATING A SELF-LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE**

HERSTELLUNG EINES PRÜFKOPFS AUF SILIZIUMBASIS ZUM PRÜFEN NACKTER HALBLEITERCHIPS

PROCEDE DE FABRICATION D'UNE INTERCONNEXION AUTO-LIMITATRICE A BASE DE SILICIUM POUR TESTER DES DES SEMI-CONDUCTEURS DENUDES

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Description

[0001] This invention relates generally to semiconductor manufacture and more particularly to methods for fabricating an interconnect suitable for testing the operability of integrated circuitry on a bare, discrete semiconductor die.

[0002] One of the fastest growing segments of the semiconductor industry is the manufacture of multi-chip modules (MCM). Multi-chip modules are being increasingly used in computers to form PC chip sets and in telecommunication items such as modems and cellular telephones. In addition, consumer electronic products such as watches and calculators typically include multi-chip modules.

[0003] With a multi-chip module, non-encapsulated dice (i.e., chips) are secured to a substrate using an adhesive. Electrical connections are then made directly to the bond pads on each die and to electrical leads on the substrate. The multi-chip module is favored because it provides significant cost and performance characteristics over packaged dice. It has been estimated that by the year 2000, 25% of all dice will be utilized in their bare or unpackaged form.

[0004] In view of the trend towards multi-chip modules, semiconductor manufacturers are required to supply unencapsulated dice that have been tested and certified as known good die (KGD). This has led to the development of test apparatus suitable for testing individual or discrete semiconductor die. As an example, test apparatus for conducting burn-in tests for discrete die are disclosed in U.S. Patent No. 4,899,107 to Corbett et al. and U.S. Patent No. 5,302,891 to Wood et al., which are assigned to Micron Technology, Inc. Other test apparatus for discrete die are disclosed in U.S. Patent No. 5,123,850 to Elder et al., and U.S. Patent No. 5,073,117 to Malhi et al., which are assigned to Texas Instruments.

[0005] With this type of test apparatus, a non-permanent electrical connection must be made between the bond pads or other contact locations on a bare, discrete die and the external test circuitry of the test apparatus. The bond pads provide a connection point for testing the integrated circuitry of the die. Bond pads on semiconductor dice are typically formed of either aluminum, gold or solder using different pad metallurgies. Furthermore, a bond pad may have a flat planar configuration or it may be formed as a raised bump.

[0006] The test apparatus for discrete die employ different techniques for making a non permanent connection to the bond pads of the die. As an example, the previously cited Wood et al. device employs a die contact member that utilizes non-bonded TAB (tape automated bonding) technology. The Elder et al. device utilizes a flexible interconnect member having an arrangement of probe bumps or members for contacting the bond pads. The Malhi et al. device uses an arrangement of cantilevered probe tips to contact the bond pads.

[0007] Alternately, non permanent wire bonding may be employed to effect the electrical connection. U.S. Patent No. 5,173,451 to Kinsman assigned to Micron Technology, Inc. describes a method in which each die is mounted in a carrier and bond wires are non permanently attached to the bond pads using ultrasonic wedge . bonding. The carrier and die are placed in the test apparatus and the bond wires are connected to external test circuitry for testing the integrated circuits on the die. Following completion of the test procedure, the temporary bond wires are separated from the bond pads and the die is separated from the carrier.

[0008] In addition to wire bonding, TAB connections and probe tips, other interconnect structures have been used to connect the bond pads on a die with the circuitry of a test apparatus. As an example, U.S. Patent No. 5,177,439 to Liu et al., describes a test apparatus that includes a probe card for making electrical contact with the bond pads of a die. The probe card is an interconnection structure formed of a semiconducting material such as silicon. The Liu probe card includes pointed silicon protrusions coated with a conductive film for contacting the bond pads. U.S. Patent No. 5,207,585 to Byrnes et al. describes an interconnect structure formed as a flexible pellicle having electrodes for making a temporary connection with bond pads formed as a flat pad or as a conductive bump.

[0009] Regardless of which bond pad connection technique is employed, it is desirable to effect a connection that causes as little damage as possible to the bond pad. If the temporary connection to a bond pad damages the pad, the entire die may be rendered as defective. This is difficult to accomplish because the connection must also produce a low resistance or ohmic contact with the bond pad. A bond pad typically includes a metal oxide layer that must be penetrated to make an ohmic contact. Some prior art interconnect structures, such as probe cards, scrape the bond pads which wipes away this oxide layer and causes excessive damage to the bond pads. Probe tips may pierce both the oxide layer and the metal bond pad and leave a deep gouge. Other interconnect structures, such as probe bumps, may not even pierce the oxide layer preventing the formation of an ohmic contact.

[0010] Another important consideration in KGD testing is the effect of thermal expansion during the test procedure. During burn-in testing, a die is heated to an elevated temperature. This causes thermal expansion of the die and test fixture. If the bond pads and the interconnect structure expand by a different amount, stress may develop between these components and adversely effect the electrical connection there between. This may also lead to excessive damage of bond pads.

[0011] In general, current physical testing apparatus for testing discrete semiconductor die have become the limiting factor in providing KGD at optimal yields. As is apparent, improved testing methods and structures for discrete die are needed in the art that are cost effective and that can be incorporated into the existing technolo-

gy of large scale semiconductor manufacture.

[0012] United States patent no. 5326428 discloses a method of engaging electrically conductive test pads on a semiconductor substrate having integrated circuitry for operability testing thereof which includes: a) providing an engagement probe having an outer surface comprising a grouping of a plurality of electrically conductive projecting apexes positioned in proximity to one another to engage a single test pad on a semiconductor substrate; (b) engaging the grouping of apexes with the single test pad on the semiconductor substrate; and (c) sending an electric signal between the grouping of apexes and test pad to evaluate operability of intergrated circuitry on the semiconductor substrate.

[0013] Further disclosed is a method of fabricating the engagement probe wherein raised contact members having projecting apexes are formed on a substrate and coated with a metal by electroplating or electroless plating.

[0014] Accordingly, it is an object of the present invention to provide an improved method for fabricating temporary interconnects for testing discrete semiconductor dice. It is a further object of the present invention to provide an improved method for fabricating temporary interconnects that is compatible with large scale semiconductor manufacture and that provides an improved interconnect structure. It is yet another object of the present invention to provide an improved method for fabricating temporary interconnects that are characterized by contact members having a conductive tip and a low resistance conductive trace for connection to external test circuitry.

[0015] In accordance with the present invention, a method of fabricating an interconnect suitable for use in testing bare, discrete semiconductor dice is provided according to claim 1. The interconnect includes a substrate having projecting contact members adapted to contact bond pads or other contact locations on a die. The contact members are formed on the substrate in a pattern that matches the size and spacing of the bond pads on the die. The tip of each contact member is covered with a conductive layer. The conductive layer is a silicide. Conductive traces or runners are formed in electrical contact with the conductive layer. Bond wires may be attached to the conductive traces to provide a conductive path to external test circuitry. In addition, the tip of each contact member includes one or more raised projections covered with the conductive layer and adapted to pierce the bond pads of the die to establish an ohmic contact. In an illustrative embodiment the raised projections are formed as sharpened blades or knife edges. The penetration depth of the raised projections into the bond pad is self-limiting by the dimensions and structure of the contact members and raised projections. Specifically, a top surface of the contact members acts as a penetration stop plane for the raised projections.

[0016] The method of the invention, generally stated, comprises a method for forming the contact members, the conductive layer on the tips of the contact members and the conductive traces to the conductive layer.

[0017] For forming the silicide conductive layer, a silicon containing layer (e.g., polysilicon, amorphous silicon) and a metal layer (e.g., platinum, titanium) are deposited on the contact member and reacted to form a silicide (e.g., PtSi2, TiSi2). The silicon containing layer and the metal layer are then removed by etching selectively with respect to the silicide layer. In a preferred embodiment, following formation of the silicide layer, a conductive layer (e.g., aluminum) is deposited (making contact to the silicide layer) and patterned to form the conductive traces.

[0018] Preferably a large number of interconnects are formed on a single substrate or wafer. This substrate can then be diced (e.g., saw cut) to singulate the interconnects.

[0019] The method of the invention stated in detail comprises the steps of: forming an array of raised contact members on a substrate each having a projecting apex (e.g., knife edge, pointed projection) for penetrating a bond pad of the die; forming a silicon containing layer on the substrate; forming an insulating layer over the silicon containing layer; removing the second insulating layer on the contact member to expose the underlying silicon containing layer; depositing a metal layer on the contact members and substrate; reacting the metal layer with the silicon containing layer to form a silicide layer; selectively etching the metal layer selective to the silicide layer to leave the contact member covered by the silicide layer; removing the insulating layer and etching the silicon containing layer selective to the silicide layer; and forming conductive traces in contact with the silicide layer.

[0020] One advantage of this process is that it allows the contact members to be easily formed with a self aligned, low resistivity silicide layer. In addition, this process employs standard photoresist patterning methods, providing simplicity and cost reduction. Furthermore, the conductive traces to the silicide layer have a low resistivity. Other objects, advantages and capabilities of the present invention will become more apparent as the description proceeds.

[0021] Figure 1 is a schematic cross sectional view of a portion of a semiconductor substrate, showing an initial process step for forming an interconnect in accordance with an embodiment of the invention;

[0022] Figure 2 is a schematic cross sectional view of the substrate showing another step of an embodiment of the method of the invention;

[0023] Figure 3 is a plan view of Figure 2;

[0024] Figure 4 is a schematic cross sectional view of the substrate showing another step in an embodiment of the method of the invention;

[0025] Figure 5 is a schematic cross sectional view of the substrate showing another step in an embodiment of the method of the invention;

[0026] Figure 6 is a plan view of Figure 5;

[0027] Figure 7 is a schematic cross sectional view of the substrate showing another step in an embodiment of the method of the invention;

[0028] Figure 8 is a schematic cross sectional view of the substrate showing another step in an embodiment of the method of the invention;

[0029] Figure 9 is a schematic perspective view showing another step in an embodiment of the method of the invention illustrating partially completed contact members;

[0030] Figure 10 is a schematic cross sectional view showing another step in an embodiment of the method of the invention for forming a conductive silicide layer on the tip on the contact member;

[0031] Figure 11 is a schematic cross sectional view showing another step in the formation of the silicide layer;

[0032] Figure 12 is a schematic cross sectional view showing another step in the formation of the conductive silicide layer;

[0033] Figure 13 is a schematic cross sectional view showing another step in the formation of the silicide layer;

[0034] Figure 14 is a schematic cross sectional view showing the completed contact member and conductive traces;

[0035] Figure 15 is a schematic cross sectional view showing an interconnect constructed using a method in accordance with an embodiment of the invention in electrical contact with the bond pads of a semiconductor die during testing of the die;

[0036] Figure 16 is a schematic cross sectional view showing an alternate embodiment of the completed contact member and conductive traces; and

[0037] Figure 17 is a plan view of the completed interconnect with a die superimposed thereon.

[0038] Referring now to Figure 1, a detailed embodiment of the process for forming an interconnect 10 for testing discrete semiconductor die is shown. The interconnect 10 includes a substrate 12 formed of a semiconducting material such as monocrystalline silicon. The substrate 12 includes a planar outer surface 14 having a mask layer 16 of a material such as silicon nitride (Si_3N_4) formed thereon. A typical thickness for the mask layer 16 is about 500Å to 3000Å (10Å = 1nm). The mask layer 16 may be formed using a suitable deposition process such as CVD.

[0039] Next, as shown in Figure 2, the mask layer 16 is patterned and etched selective to the substrate 12 to form a hard mask that includes masking blocks 18, 20, 24 and 26. Depending on the materials used for the mask layer 16 this etch step may be performed using a wet or dry etch. As an example, a layer of silicon nitride may be etched using hot (e.g., 180°C) phosphoric acid.

[0040] As shown in the plan view of Figure 3, the masking blocks 18, 20, 24 and 26 are formed in a parallel spaced array and are sized and shaped to fit within the perimeters of a generally rectangular or square shaped bond pad of a semiconductor die (e.g., 100μm x 100μm). As is apparent, such a parallel spaced array is merely exemplary and other configurations are possible. Other suitable arrangements for the masking blocks include enclosed rectangles, squares triangles, T-shapes and X-shapes.

[0041] Next, as shown in Figure 4, a wet or dry isotropic or anisotropic etch process is used to form projecting apexes 40, 42, 44, 46 on the substrate. For an anisotropic etch, in which the etch rate is different in different directions, an etchant solution containing a mixture of KOH and H_2O may be utilized. This isotropic etch results in the formation of triangular tips as shown in Figure 5. This is a result of the different etch rates of monocrystalline silicon along the different crystalline orientations. For an isotropic etch, in which the etch rate is the same in all directions, an etchant solution containing a mixture of HF, HNO_3 and H_2O may be utilized.

[0042] Alternately, in place of an isotropic or anisotropic etch process, the substrate may be subjected to an oxidizing atmosphere to oxidize portions of the substrate 12 not covered by the masking blocks 18, 20, 24, 26, of the mask layer 16. As an example, the oxidizing atmosphere may comprise steam and O_2 at an elevated temperature (e.g. 950°C). The oxidizing atmosphere oxidizes the exposed portions of the substrate 12 and forms an insulating layer 49 (e.g., silicon dioxide). At the same time, projecting apexes 40, 42, 44 and 46 are formed under the masking blocks. The projecting apexes 40, 42, 44, 46 may also be formed by a deposition process out of a different material than the substrate 12.

[0043] Next, as shown in Figure 5, the masking blocks 18, 20, 24, 26 are stripped using a wet etchant such as H_3PO_4 that is selective to the substrate 12. With an oxidizing process the insulating layer 49 is stripped using a suitable wet etchant such as HF.

[0044] Thus as shown in to Figure 6, the steps of patterning and etching and stripping form projecting apexes 40, 42, 44, 46 which are in the form of parallel spaced knife edges. The projecting apexes 40, 42, 44, 46 form an apex group 43 which has an overall peripheral dimension which falls within the boundaries of a generally rectangular or square bond pad of a semiconductor die. Although multiple knife edges are formed for each bond pad, it is to be understood that a single knife edge per bond pad would also be suitable.

[0045] The projecting apexes 40, 42, 44, 46 project from a surface 56 of the substrate 12 and include tips 58 and bases 60. Bases 60 of adjacent projecting apexes 40, 42, 44, 46 are spaced from one another a distance sufficient to define a penetration stop plane 62 there between. Example spacing between apexes would be 10 μm, while an example length of an individual stop plane 62 would be from 3 to 10 μm. The function of the penetration stop plane 62 will be apparent from the continuing discussion. The tip 58 and base 60 of each projecting apex 40, 42, 44, 46 are spaced apart by

a protecting distance that is preferably about one-half the thickness of a bond pad on a semiconductor die. As an example, this projecting distance will be on the order of .5 to 1 μm. Subsequent to formation of the projecting apexes 40, 42, 44, 46, 48 additional etching may be used to further sharpen the apexes 40, 42, 44, 46.

[0046] Next, as shown in Figure 7, all of the projecting apexes 40, 42, 44, 46 in apex group 43 are covered with a nitride masking layer 64 and photopatterned. Then as shown in Figure 8, the substrate 12 is etched around the masking layer 64 to form raised contact members 65. Typical etching techniques comprise wet anisotropic etching with a mixture of KOH:H_2O. This type of etching is also known in the art as bulk micro-machining. The contact members 65 are sized and shaped to contact a bond pad of a semiconductor die. Each contact member 65 viewed from above has a generally square rectangular peripheral configuration and is dimensioned to fall within the perimeter of a bond pad. The contact members 65 can also be formed in other peripheral configurations such as triangles, polygons or circles. The height of each contact member 65 will be on the order of 50-100 μm and the width on each side about 40-80 μm. Figure 9 shows two adjacent contact members 65a and 65b extending from the substrate. The spacing of the contact members 65a and 65b matches the spacing of adjacent bond pads on a semiconductor die (e.g., 50 to 100μm).

[0047] The method of the invention forms a conductive silicide layer 78A (Figure 14) on the tip of each contact member 65. In addition, conductive traces 80 (Figure 14) are formed to provide a conductive path to the silicide layer 78A (Figure 14). A detailed embodiment of this segment of the process is illustrated in Figures 10-14.

[0048] Initially, as shown in Figure 10, an insulating layer 68 (e.g., SiO_2), is formed on the substrate 12 and contact members 65. The insulating layer 68 is formed by oxidation of the substrate 12 and may be accomplished by exposing the substrate 12 and to an oxidizing atmosphere for a short time. SiO_2 can also be deposited using CVD. Another commonly used insulator suitable for this purpose is Si_3N_4.

[0049] As also shown in Figure 10, a silicon containing layer such as polysilicon layer 70 is formed on the insulating layer 68. The polysilicon layer 70 is required to form a silicide with a metal layer 78 (Figure 13) during subsequent processing. The polysilicon layer 70 may be formed of doped or undoped polysilicon. Alternately, other silicon containing layers such as doped or undoped amorphous silicon may be employed in place of polysilicon. However, polysilicon is preferred for most applications because of lower resistivity and better electrical and structural properties and because it lends itself to simpler etching processes. The polysilicon layer 70 may be deposited on the insulating layer 68 using a suitable deposition process such as chemical vapor deposition (CVD) or by using an epitaxial growth process. A typical thickness for the polysilicon layer 70 would be from about 500Å to 3000Å.

[0050] Next, as shown in Figure 11, a second insulating layer 72 (e.g., SiO_2) is formed on the polysilicon layer 70. The second insulating layer 72 may be deposited using CVD techniques or formed by exposing the polysilicon layer 70 to an oxidizing environment. A typical thickness for the second insulating layer 72 would be from about 500Å to 3000Å.

[0051] Next, as shown in Figure 12, a layer of photoresist 74 is formed on the substrate 12 by spin-on or other suitable deposition process. The photoresist 74 is then developed such that the contact members 65 are exposed. This is relatively easy to accomplish because the photoresist 74 will tend to puddle on the lower portions of the structure, such as surface of the substrate 12, leaving the projecting contact members 65 exposed.

[0052] Following development of the photoresist 74, the second insulating layer 72 (Figure 11) on the contact member 65 is removed leaving the polysilicon layer 70 exposed on the tip of the contact member 65. This may be accomplished using a dry etch process with a chlorine or fluorine based etchant such as CF_4, CHF_3, C_2F_6, or C_3F_8.

[0053] Next, as shown in Figure 13, the photoresist 74 is removed and a metal layer 78 is deposited on the exposed polysilicon layer 70. The metal layer 78 covers the polysilicon layer 70 on the tip and sidewalls of the contact member 65 and completely covers the apex group 43. In addition, the metal layer 78 covers the second insulating layer 72 on the substrate 12. The metal layer 78 can be deposited to a thickness of about 500Å to 3000Å using a suitable deposition process such as low pressure chemical vapor deposition (LPCVD), or using standard metal sputtering or evaporation techniques.

[0054] The metal layer 78 is formed of a metal that will react with the polysilicon layer 70 to form a metal silicide. Suitable metals include the refractory metals, such as titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt) and molybdenum (Mo). In general, silicides of these metals (WSi2, $TaSi_2$, $MOSi_2$, $PtSi_2$ and $TiSi_2$) are formed by alloying with a silicon surface. Other suitable metals include cobalt (Co), nickel (Ni), molybdenum (Mo), copper (Cu), gold (Au) and iridium (Ir).

[0055] Following deposition of the metal layer 78, a sintering process is performed in which the metal layer 78 is heated and reacts with the polysilicon layer 70 to form a silicide. This type of sintering process is also known in the art as salicide sintering. Such a salicide sintering step can be performed by heating the polysilicon layer, 70 and metal layer 78 to a temperature of about 650° to 820°C for typical thicknesses in thousands of angstroms (e.g., 2000Å - 3000Å). This sintering process can be performed in one single step or using multiple temperature steps. A silicide layer 78A forms at the interface of the metal layer 78 and the polysilicon layer 70.

[0056] Next, as shown in Figure 14, the unreacted

portions of the metal layer 78 and the polysilicon layer 70 are removed while the silicide layer 78A is left at the tip of the contact member 65. This can be done by etching the metal layer 78 and the polysilicon layer 70 selective to the silicide layer 78A. By way of example for $TiSi_2$, for etching the unreacted portion of a titanium metal layer 78, a wet etchant such as a solution of ammonia and hydrogen peroxide, or a H_2SO_4, H_2O_2 mixture, that will attack the metal layer 78 and not the silicide layer 78A, can be used. Alternately, a dry etch process with an etchant species such as Cl_2 or BCl_3 can be used to etch the metal layer 78 selective to the silicide layer 78A.

[0057] For etching the unreacted portion of the polysilicon layer 70 selective to the silicide layer 78A, a wet etchant such as an $HF:HNO_3:H_2O$ acid mixture (typical ratios of 1:10:10) can be used to remove the unreacted portion. A wet isotropic etchant can also be used for this purpose. Alternately the polysilicon layer 70 may etched selective to the silicide layer 78A using a dry etch process and an etchant such as NF_3 at low pressures (typically 30m torr) or CL_2 and HBr at 130 m torr. The remaining second insulating layer 72 on the substrate 12 needs to be etched away prior to the polysilicon etch described above. This can be accomplished using a dry etch process as previously described. As shown in Figure 14, the completed interconnect 10 includes the silicide layer 78A which covers the tip of the contact member 65 and the apex group 43 and a portion of the sidewalls of the contact member 65. Alternately, the silicide layer 78A can be extended to cover part of the base of the contact member 65 as shown in Figure 16.

[0058] The resistivity of the silicide layer 78A may be lowered using an annealing process. This may be accomplished by heating the substrate 12 and silicide layer 78A to a temperature of between about 780°C to 850°C for several minutes.

[0059] As also shown in Figure 14, conductive traces 80 are formed on the substrate 12 to provide a conductive path in electrical contact with the silicide layer 78A. The conductive traces 80 are formed by depositing and etching a second metal layer comprising a highly conductive metal such as aluminum, copper or alloys thereof, or a refractory metal such as titanium, tungsten, tantalum and molybdenum or alloys of these metals. Other conductive materials such as polysilicon may also be employed to form the conductive traces 80. The conductive traces 80 may be formed using a standard metallization process such as a blanket CVD deposition or sputtering followed by photopatterning and etching. As an example, a wet etchant such as H_3PO_4 can be used to etch a patterned aluminum layer selectively from desired areas on substrate 12 to form aluminum conductive traces 80.

[0060] Figure 17 shows an exemplary layout for the conductive traces 80 and contact members 65 in the completed interconnect 10. Such a layout will depend on the bond pad configuration of a die under test. Preferably a large number of interconnects 10 can be formed using semiconductor circuit fabrication techniques on a single substrate or wafer (not shown). The wafer can then be sawed (i.e., diced) to singulate the interconnects 10.

[0061] Referring back again to Figure 14, bond wires 82 are wire bonded to the conductive traces 80 utilizing a conventional wire bonding process (e.g., solder ball) to provide a conductive path from the completed interconnect 10 to external test circuitry. As shown in Figure 17, each conductive trace includes a bonding site 92 for wire bonding the bond wires 82. In place of a wire bonding process other conductive paths such as external connector pads, slide connectors and other mechanical connector arrangements may be utilized (not shown).

[0062] Referring now to Figure 15, the interconnect 10 is shown engaging a semiconductor die 85 as a die under test (DUT). The die 85 includes a substrate 86 and an arrangement of exposed bond pads 88. A protective layer 90 covers the die 85 such that only the bond pads 88 are exposed. The bond pads 88 have a thickness of "A" and may be covered by a thin layer of oxide (not shown) depending on the metallization used for the bond pads.

[0063] In use of the interconnect 10, the projecting apexes 40, 42, 44, 46, represented by apex group 43 of a contact member 65, pierce the bond pad 88 and its oxide coating. The penetration of the apex group 43 is limited by the stop plane 62 (Figure 8) formed by the surface of the contact member 65. The force required to press the apex group 43 into the bond pad 88 can also be monitored as an indication of the penetration depth. Optimally, the apex group 43 extends about half way through the thickness of the bond pad 88 (i.e., 1/2 of the distance A in Figure 15). This provides a low resistance ohmic contact between the silicide layer 78A and the bond pad 88. At the same time a penetration depth into the bond pad 88 is limited by the dimensions of the projecting apexes 40, 42, 44, 46 and by the stop plane provided by the top surface of the raised constant member 65.

[0064] The conductive trace 80 and bond wire 82 provide a connection from the silicide layer 78A to test circuitry for testing the die 85. As an example, the opposite end of the bond wire 82 may be connected to a temporary holder for the die 85 adapted to be placed along with the interconnect 10 in a test apparatus (not shown). The test apparatus may include a connection to the temporary holder and to test circuitry. Such an arrangement is described in more detail in U.S. No. 5,302,891 entitled "Discrete Die Burn-In For Non-Packaged Die".

[0065] Thus the invention provides a method for forming an interconnect useful in establishing an electrical connection to the bond pads of a semiconductor die for testing and other purposes. Although preferred materials have been described, it is to be understood that other materials may also be utilized. Furthermore, although the method of the invention has been described with reference to certain preferred embodiments, as will be ap-

parent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

Claims

1. A method of fabricating an interconnect for testing a semiconductor integrated circuit die comprising:

   forming an array of raised contact members (65) on a substrate (12) said contact members (65) sized and spaced to engage electrically conductive contact locations on the die;

   wherein the contact members include a projecting apex (40, 42, 44, 46) adapted to pierce the contact locations on the die to establish an ohmic contact;

   forming a silicon containing layer (70) of material on the contact members (65) and on the substrate (12) in the regions between the contact members;

   selectively forming an insulating layer (72) on said silicon containing layer (70) in the regions between the contact members;

   forming a metal layer (78) on the contact members (65) and in the regions between the contact members;

   reacting the silicon containing layer (70) with the metal layer (78) to form a silicide layer (78A) on the contact members (65);

   etching the remaining unreacted portions of the metal layer (78) selective to the silicide layer (78A) followed by removing the insulating layer (72) and then etching the remaining unreacted portions of the silicon containing layer (70) selective to the silicide layer; and

   forming conductive traces (80)on the substrate in contact member comprises the steps of:

      forming an insulating layer (72) on the silicon containing layer (70);

      forming a mask (74) in the regions between the contact members, leaving the contact members (65) exposed;

      removing the insulating layer (72) on the contact members (65); and

      removing the mask.

   contact with the silicide layer (78A).

2. The method as recited in claim 1 and wherein the silicon containing layer (70) and the metal layer (78) are heated to form the silicide layer (78A).

3. The method as recited in claim 1 and wherein the silicon'containing layer (70) is selected from the group of materials consisting of polysilicon and amorphous silicon.

4. The method as recited in claim 1 and wherein the metal layer (78) is selected from the group of materials consisting of titanium, platinum, tungsten, cobalt, tantalum, nickel, molybdenum, copper, gold and iridium.

5. The method as recited in claim 1 and wherein the projecting apex (40, 42, 44, 46) is formed as a knife edge adapted to pierce the bond pads (88) and to provide a stop plane to limit penetration into the bond pads (88).

6. The method as recited in claim 1 and wherein the substrate (12) comprises monocrystalline silicon having an insulating layer (68) formed on a surface thereof.

7. The method as recited in claim 1 and further comprising annealing the silicide layer (78A) to lower its resistivity.

8. The method as recited in claim 1 and further comprising attaching bond wires (82) to the conductive traces (80).

9. The method as recited in claim 1 and further comprising forming a plurality of interconnects (10) on a single substrate and then singulating the interconnects.

10. The method as recited in claim 1 and wherein the conductive traces (80) are formed by a metallization process from a metal selected from the group consisting of aluminum, copper, platinum, titanium, tungsten, tantalum, molybdenum and alloys of these metals.

11. The method as recited in claim 1 and further comprising placing the interconnect (10) in a test apparatus for establishing a temporary electrical connection between the die and test circuitry.

12. The method as recited in claim 1, wherein the step of selectively forming an insulating layer on said silicon containing layer in the regions between the contact member comprises the steps of :

    forming an insulating layer (72) on the silicon containing layer (70);

    forming a mask (74) in the regions between the contact members, leaving the contact members (65) exposed;

    removing the insulating layer (72) on the contact members (65); and

    removing the mask.

Patentansprüche

1. Verfahren zur Herstellung einer Verdrahtung zum Testen eines Halbleiter-Chips mit einer integrierten Schaltung, umfassend:

   das Ausbilden einer Anordnung erhabener Kontaktelemente (65) auf einem Substrat (12), wobei die Kontaktelemente (65) eine solche Größe und einen solchen Abstand zueinander aufweisen, dass sie an elektrisch leitende Kontaktstellen auf dem Chip angreifen;
   worin die Kontaktelemente eine vorragende Spitze (40, 42, 44, 46) umfassen, die dazu ausgebildet ist, die Kontaktstellen auf dem Chip zu durchdringen, um einen ohmschen Kontakt herzustellen;

   das Ausbilden einer siliziumhältigen Schicht (70) aus Material auf den Kontaktelementen (65) und auf dem Substrat (12) in den Bereichen zwischen den Kontaktelementen;

   das selektive Ausbilden einer Isolierungsschicht (72) auf der siliziumhältigen Schicht (70) in den Bereichen zwischen den Kontaktelementen;

   das Ausbilden einer Metallschicht (78) auf den Kontaktelementen (65) und in den Bereichen zwischen den Kontaktelementen;

   das Reagieren lassen der silikonhältigen Schicht (70) mit der Metallschicht (78), um auf den Kontaktelementen (65) eine Silicidschicht (78A) auszubilden;

   das Ätzen der verbleibenden unreagierten Abschnitte der Metallschicht (78) selektiv bezüglich der Silicidschicht (78A), gefolgt vom Entfernen der Isolierungsschicht (72) und dann dem Ätzen der (freiliegenden) unreagierten Abschnitte auf der silikonhältigen Schicht (70) selektiv bezüglich der Silicidschicht; und

   das Ausbilden von Leiterzügen (80) auf dem Substrat in Kontakt mit der Silicidschicht (78A).

2. Verfahren nach Anspruch 1, worin die siliziumhältige Schicht (70) und die Metallschicht (78) erwärmt werden, um die Silicidschicht (78A) zu bilden.

3. Verfahren nach Anspruch 1, worin die siliziumhältige Schicht (70) aus der Gruppe von Materialien ausgewählt ist, die aus Polysilizium und amorphem Silizium besteht.

4. Verfahren nach Anspruch 1, worin die Metallschicht (78) aus der Gruppe von Materialien ausgewählt ist, die aus Titan, Platin, Wolfram, Cobalt, Tantal, Nikkel, Molybdän, Kupfer, Gold und Iridium besteht.

5. Verfahren nach Anspruch 1, worin die vorragende Spitze (40, 42, 44, 46) als Schneidklinge ausgebildet ist, die dazu ausgebildet ist, die Kontaktflächen (88) zu durchdringen und eine Anschlagebene bereitzustellen, um das Eindringen in die Kontaktflächen (88) zu begrenzen.

6. Verfahren nach Anspruch 1, worin das Substrat (12) monokristallines Silizium umfasst, auf dessen Oberfläche eine Isolierungsschicht (68) ausgebildet ist.

7. Verfahren nach Anspruch 1, das weiters das Ausglühen der Silicidschicht (78A) umfasst, um ihren spezifischen Widerstand zu senken.

8. Verfahren nach Anspruch 1, das weiters das Befestigen von Kontaktdrähten (82) an den Leiterzügen (80) umfasst.

9. Verfahren nach Anspruch 1, das weiters das Ausbilden einer Vielzahl von Verdrahtungen (10) auf einem einzigen Substrat und anschließend das Vereinzeln der Verdrahtungen umfasst.

10. Verfahren nach Anspruch 1, worin die Leiterzüge (80) durch ein Metallisierungsverfahren aus einem Metall gebildet werden, das aus der aus Aluminium, Kupfer, Platin, Titan, Wolfram, Tantal, Molybdän und Legierungen dieser Metalle bestehenden Gruppe ausgewählt ist.

11. Verfahren nach Anspruch 1, das weiters das Anordnen der Verdrahtung (10) in einer Testvorrichtung umfasst, um eine vorübergehende elektrische Verbindung zwischen dem Chip und einer Testschaltung herzustellen.

12. Verfahren nach Anspruch 1, worin der Schritt des selektiven Ausbildens einer Isolierungsschicht auf der siliziumhältigen Schicht in den Bereichen zwischen dem Kontaktelement die folgenden Schritte umfasst:

    das Ausbilden einer Isolierungsschicht (72) auf der siliziumhältigen Schicht (70);

    das Ausbilden einer Maske (74) in den Bereichen zwischen den Kontaktelementen, wobei die Kontaktelemente (65) freiliegend bleiben;

    das Entfernen der Isolierungsschicht (72) auf den Kontaktelementen (65); und

das Entfernen der Maske.

Revendicati ns

1. Méthode de fabrication d'une interconnexion. pour tester une matrice de circuit intégré à semi-conducteurs consistant à :

   former une série d'organes surélevés de contact (65) sur un substrat (12), lesdits organes de contact (65) dimensionnés et espacés pour engager des emplacements de contact électriquement conducteurs sur la matrice;

   où les organes de contact comprennent des sommets en protubérance (40, 42, 44, 46) adaptés à percer les emplacements de contact sur la matrice pour établir un contact ohmique;
   former une couche de matière (70) contenant du silicium sur les organes de contact (65) et sur le substrat (12) dans les régions entre les organes de contact;
   former sélectivement une couche isolante (72) sur ladite couche contenant du silicium (70) dans les régions entre les organes de contact;
   former une couche de métal (78) sur les organes de contact (65) et dans les régions entre les organes de contact;
   faire réagir la couche contenant du silicium (70) avec la couche de métal (78) pour former une couche de siliciure (78A) sur les organes de contact (65);
   attaquer les portions restantes n'ayant pas réagi de la couche de métal (78) sélective pour la couche de siliciure (78A) avec ensuite enlèvement de la couche isolante (72) puis attaque des portions exposées n'ayant pas réagi de la couche (70) contenant du silicium sélective à la couche de siliciure; et
   former des traces conductrices (80) sur le substrat en contact avec la couche de siliciure (78A).

2. Méthode selon la revendication 1 et où la couche contenant du silicium (70) et la couche de métal (78) sont chauffées pour former la couche de siliciure (78A).

3. Méthode selon la revendication 1 et où la couche contenant du silicium (70) est sélectionnée dans le groupe de matières consistant en polysilicium et silicium amorphe.

4. Méthode selon la revendication 1 et où la couche de métal (78) est sélectionnée dans le groupe de matières consistant en titane, platine, tungstène, cobalt, tantane, nickel, molybdène, cuivre, argent et iridum.

5. Méthode selon la revendication 1 et où le sommet en protubérance (40, 42, 44, 46) est formé en tant que lame de couteau adaptée à percer les plots de liaison (88) et à produire un plan d'arrêt pour limiter la pénétration dans les plots de liaison (88).

6. Méthode selon la revendication 1 et où le substrat (12) comprend du silicium monocristallin ayant une couche isolante (68) formée sur une surface de celui-ci.

7. Méthode selon la revendication 1 et comprenant de plus le recuit de la couche de silicium (78A) pour abaisser sa résistivité.

8. Méthode selon la revendication 1 et comprenant de plus l'attache de fils de liaison (82) aux traces conductrices (80).

9. Méthode selon la revendication 1 et comprenant de plus la formation d'un certain nombre d'interconnexions (10) sur un seul substrat puis la singulation des interconnexions.

10. Méthode selon la revendication 1 et où les traces conductrices (80) sont formées par un procédé de métallisation à partir d'un métal sélectionné dans le groupe consistant en aluminium, cuivre, platine, titane, tungstène, tantale, molybdène et alliages de ces métaux.

11. Méthode selon la revendication 1 et comprenant de plus la mise en place de l'interconnexion (10) dans un appareil de test pour établir une connexion électrique temporaire entre la matrice et le circuit de test.

12. Méthode selon la revendication 1, où l'étape de former sélectivement une couche isolante sur ladite couche contenant du silicium dans les régions entre l'organe de contact comprend les étapes de :

    former une couche isolante (72) sur la couche (70) contenant du silicium;
    former une masque (74) dans les régions entre les organes de contact, laissant les organes de contact (65) exposés;
    enlever la couche isolante (72) sur les organes de contact (65) ; et
    enlever le masque.

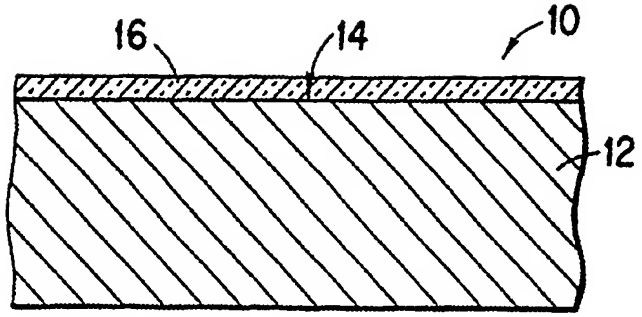


FIG. 1

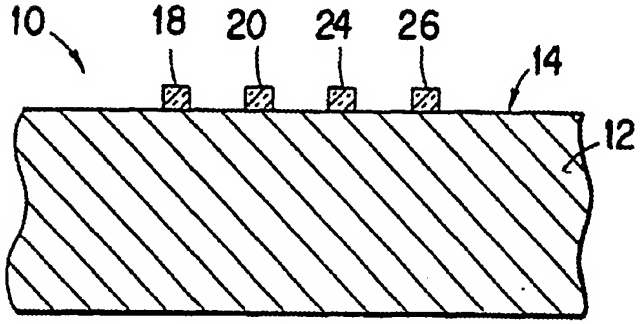


FIG. 2

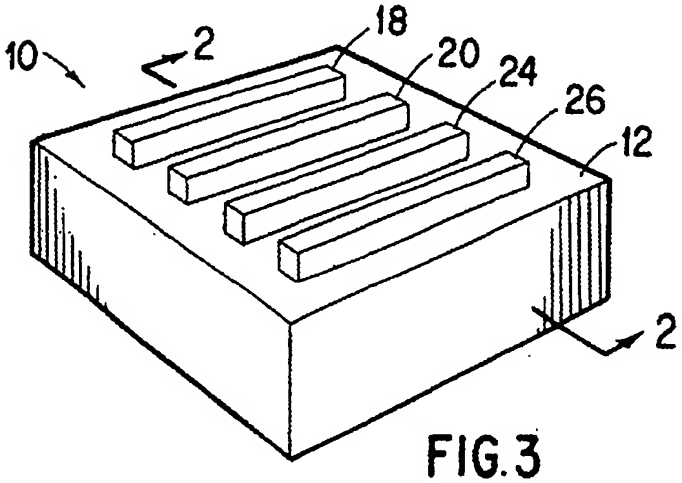


FIG. 3

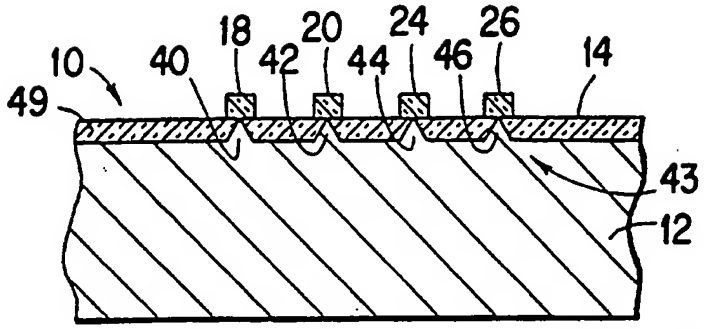


FIG. 4

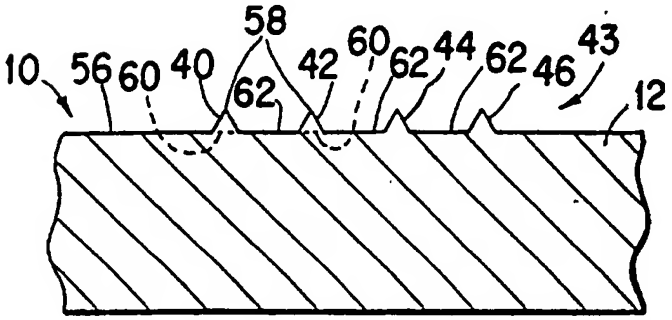
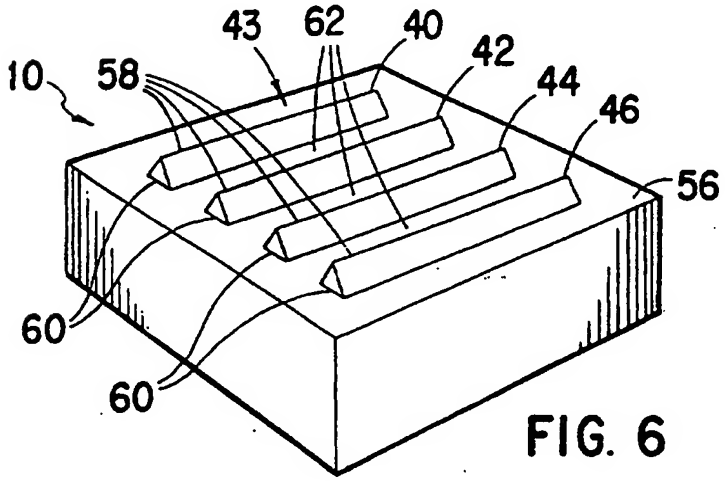


FIG. 5



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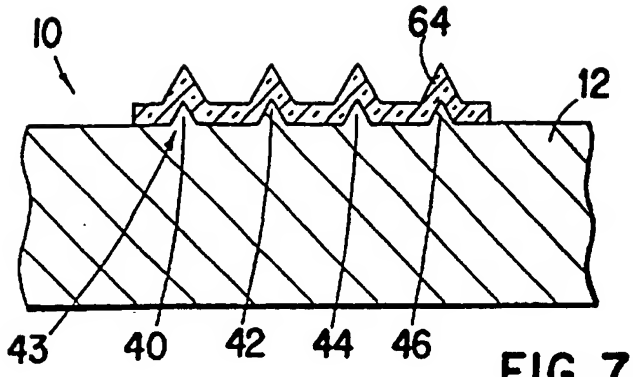

FIG. 7

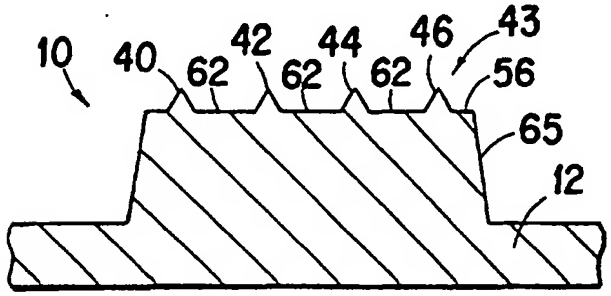

FIG. 8

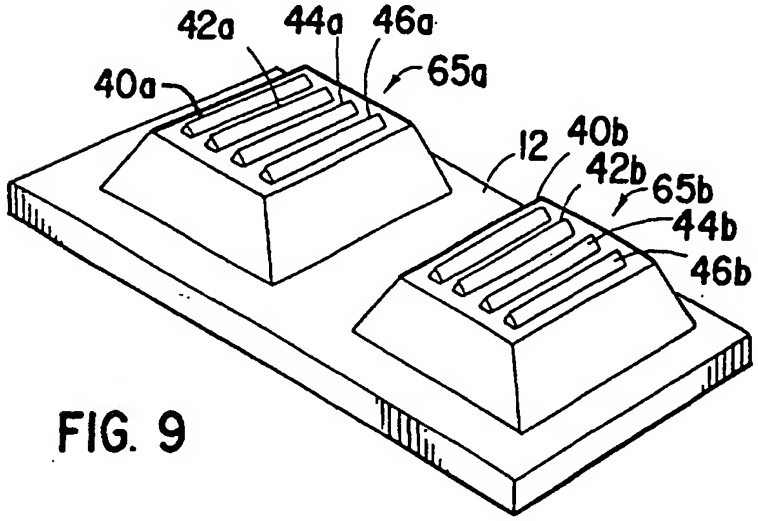

FIG. 9

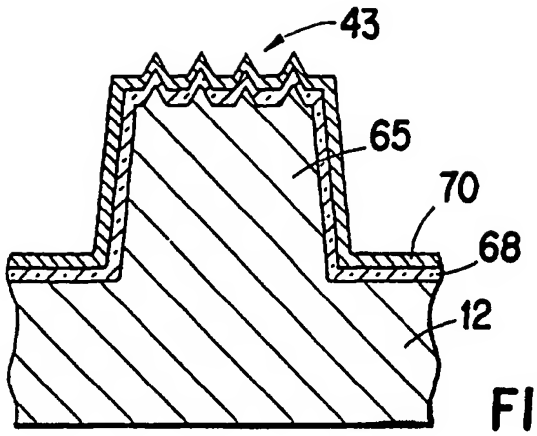

FIG. 10

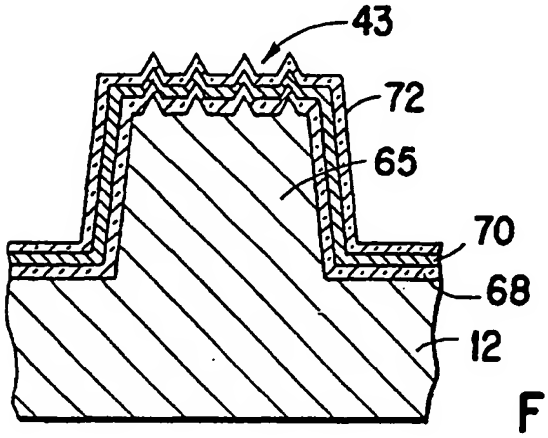

FIG. 11

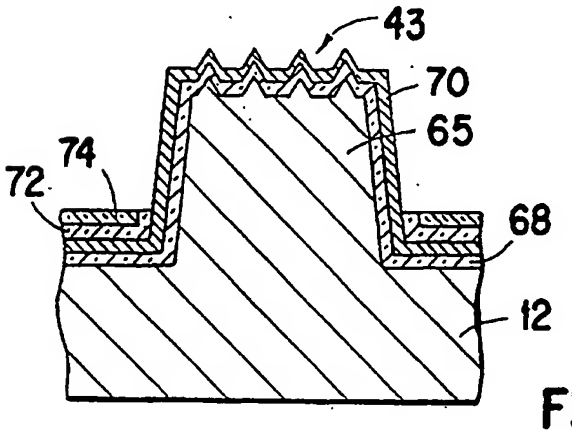

FIG. 12

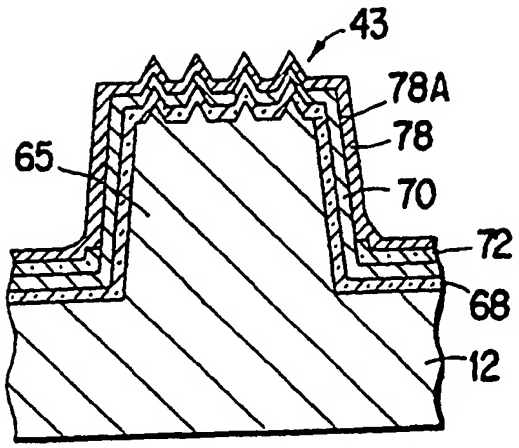

FIG. 13

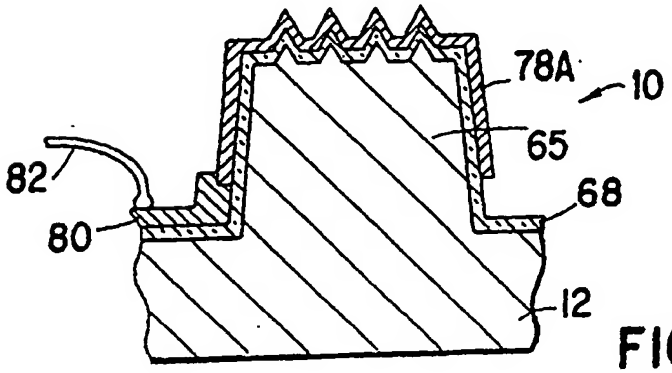

FIG. 14

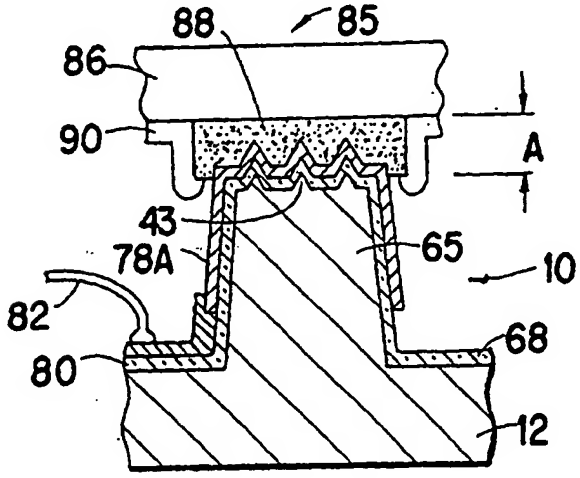

FIG. 15

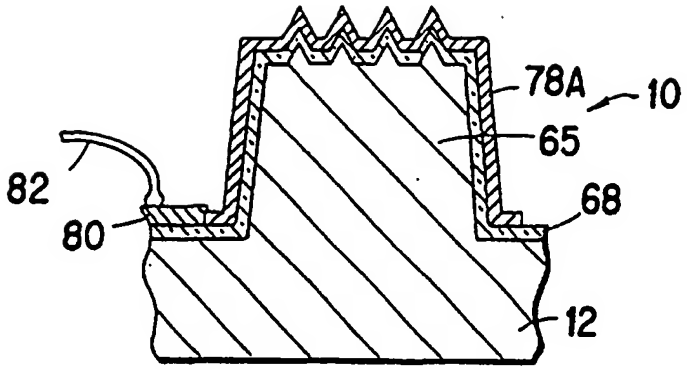

FIG. 16

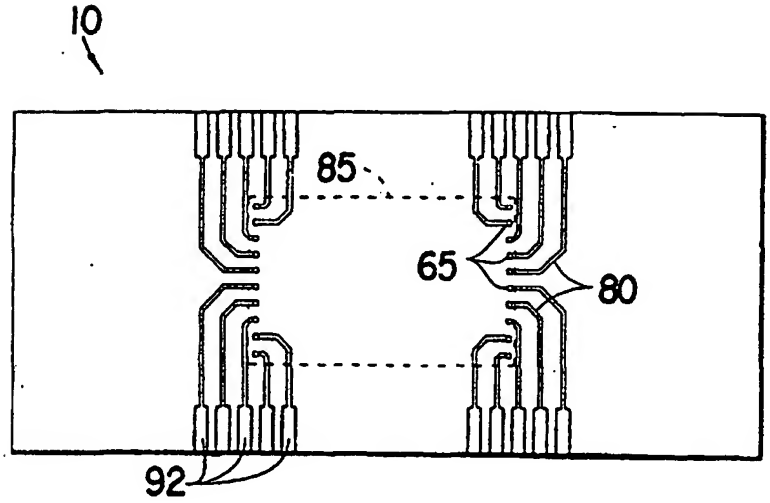

FIG. 17